In the Claims:

Amend the claims as follows:

1 (currently amended). A method for testing an integrated circuit having a power grid and a plurality of ordered connections to the power grid, comprising:

applying a time-varying input signal to the integrated circuit;

measuring a plurality of power signals produced at a plurality of respective ordered connections in response to the input signal;

identifying a defect in the integrated circuit from a combination of two or more of the power signals so measured ~~one or more defects in the integrated circuit~~.

2 (original). The method of claim 1, wherein at least that portion of the integrated circuit to be tested comprises a digital circuit.

3 (original). The method of claim 2, wherein the time-varying input signal comprises a time varying vector of logic inputs.

4 (original). The method of claim 1, wherein the measuring occurs at a first pair of the ordered connections and at a second pair of the ordered connections, the two power signals measured at each pair defining a contour of a power signal characteristic, the measuring further comprising determining the centroid of the power signal characteristic by finding the intersection of the respective contours for each pair of ordered connections.

5 (original). The method of claim 4, wherein the first pair of ordered connections and the second pair of ordered connections share a common connection.

6 (original). The method of claim 4, wherein the identifying defects comprises identifying the spatial location of at least one power signal characteristic centroid produced in response to the time-varying input signal that varies from its expected location.

7 (original). The method of claim 6, wherein the evaluating comprises comparing the location of at least one or more said power signal characteristic centroids to a standard to determine whether those locations represent defects.

8 (original). The method of claim 7, wherein the standard is an acceptable deviation from the expected location of the centroid in a reference device.

9 (original). The method of claim 8, wherein the reference device is an actual reference circuit.

10 (original). The method of claim 8, wherein the reference device is a simulated reference circuit.

12 (original). The method of claim 7, wherein the measuring signals comprises measuring currents and the power signal characteristic is a current characteristic.

13 (original). The method of claim 12, wherein the measuring signals includes integrating the measured currents over a measurement period to produce measured power signals.

14 (original). The method of claim 7, wherein the measuring signals comprises measuring voltages and the power signal characteristic is a voltage characteristic.

15 (original). The method of claim 14, wherein the measuring signals includes integrating the measured voltages over a measurement period to produce measured power signals.

16 (original). The method of claim 7, wherein the measuring signals includes performing a time-frequency Fourier transform on the signals to produce frequency-domain representations thereof and the power signal characteristic is a frequency-domain characteristic.

17 (original). The method of claim 16, wherein the measuring signals includes integrating the frequency-domain representations over a measurement band to produce measured signals.

18 (original). The method of claim 1, wherein the measuring signals comprises measuring currents.

19 (original). The method of claim 18, wherein the measuring signals includes integrating the measured currents over a measurement period to produce respective integrated current areas.

20 (original). The method of claim 19, wherein the measuring occurs at a first pair of the ordered connections and at a second pair of the ordered connections, the two integrated current areas measured at each pair defining respective contours of current areas, the measuring further comprising determining the centroid of current area by finding the intersection of the contours for each pair of ordered connections.

21 (original). The method of claim 20, wherein the set of locations for the first pair of ordered connections is at least a portion of the locus of points of a first hyperbola, the set of locations for the second pair of ordered connections is at least a portion of the locus of points of a second hyperbola.

22 (original). The method of claim 21, wherein at least that portion of the integrated circuit to be tested comprises a digital circuit.

23 (original). The method of claim 22, wherein the time-varying input signal comprises a time varying vector of logic inputs.

24 (original). The method of claim 21, wherein the first pair of ordered connections and the second pair of ordered connections share a common connection.

25 (original). The method of claim 21, wherein the identifying defects comprises identifying the spatial location of at least one integrated current area centroid produced in response to the time-varying input signal that varies from its expected location.

26 (original). The method of claim 25, wherein the evaluating comprises comparing the location of one or more said integrated current area centroids to a standard to determine whether those locations represent defects.

27 (original). The method of claim 26, wherein the standard is an acceptable deviation from the expected location of the centroid in a reference device.

28 (original). The method of claim 27, wherein the reference device is an actual reference circuit.

29 (original). The method of claim 27, wherein the reference device is a simulated reference circuit.

30 (original). The method of claim 24, further comprising determining a test current fraction of current area measured at the common connection for each pair of connections relative to the total current area measured for both connections thereof in response to the time varying input signal and determining the respective hyperbolic contours therefore.

31 (original). The method of claim 30, further comprising, without applying the time varying input signal:

injecting a calibration signal in the integrated circuit at the location of said common connection;

measuring currents drawn at each of the connections of the first and second pairs of connections in response to the preceding step;

injecting a calibration signal in the integrated circuit at the location of the non-common connection of the first pair of connections;

measuring the currents drawn at the connections of the first pair of common connections in response to the preceding step;

injecting a calibration signal in the integrated circuit at the location of the non-common connection of the second pair of connections;

measuring the currents drawn by the second pair of connections in response to the preceding step;

for each of the two pairs of connections, determining the calibration current fraction responsive to a calibration signal that is drawn at each connection of each pair of connections when the calibration signal is injected at the location of each connection of the pair; and

determining the hyperbola parameters for each pair of connections in response to the time varying input using the test current fractions and corresponding calibration current fractions to find the hyperbolic contours.

32 (original). The method of claim 31 wherein, prior to computing test current fractions and calibration current fractions for the integrated circuit under test, all current areas are also measured for a reference device, the ratios of test current areas to calibration current areas are computed, those ratios are multiplied times the calibration current areas measured for the circuit under test, the products are subtracted from the respective test current areas for the circuit under test, and the respective differences are used to compute the current fractions which are employed to find the hyperbolic contours, and the intersection of the hyperbolic contours is taken to be the location of a defect.

33 (original). The method of claim 31, further comprising, prior to computing the test and current fractions:

determining a first two-dimensional array of reference calibration current areas for a reference device, one dimension of the array corresponding to the ordered connection at which a calibration current is measured and the other dimension of the array corresponding to the ordered connection at whose location a calibration signal is injected;

determining a second two-dimensional array of test device calibration current areas for the integrated circuit under test, one dimension of the array corresponding to the ordered connection at which a calibration current is measured and the other dimension of the array corresponding to the ordered connection at whose location a calibration signal is injected;

inverting the second array and multiplying it times the second array to produce a third, transformation array;

multiplying the measured test current areas for the first and second pairs of connections times the corresponding sub array of the transformation array to prior to computing the test current fractions; and

using the reference device calibration current areas to instead of the test device calibration current areas to determine the calibration current fractions.

34 (original). The method of claim 1, further comprising determining from the power signal measurements the location of said one or more defects so identified.

35 (cancelled).

36 (currently amended). A system for testing an integrated circuit having a power grid and a plurality of ordered connections to the power grid, comprising:

a probe for connecting to the die of an integrated circuit prior to final packaging, the probe including a power supply for the die;

a data acquisition device, coupled to the probe, for applying transient input signals to the die and acquiring a plurality of die power signal measurements from respective ordered connections in response thereto; and

a data processor, coupled to the data acquisition device, for determining whether a combination of two or more of the power signal measurements indicates the presence of a defect in the die.

37 (original). The system of claim 36, wherein the data processor determines whether the integrated circuit is defective by identifying from the power signal measurements one or more potential power signal anomalies, and evaluating the power signal anomalies to determine whether they are due to a defect in the integrated circuit.

38 (original). The system of claim 36, wherein the data processor determines the location of a defect based on the simultaneous solution of a plurality of parametric equations whose parameters include measured die power signals.

39 (original). The system of claim 36, wherein the data acquisition device is adapted to acquire calibration power signals from the integrated circuit and the data processor is adapted to transform the power signal measurements to a reference device space using the calibration power signals so as to reduce the effects of probe connection contact resistance.

40 (cancelled).